REMARKS

Claims 1 - 38 are pending in the present application, of which claims 3, 4, 6-27, 29-32, 34, 35, 37 and 38 have been withdrawn from consideration. By this Amendment, claims 1, 28 and 33 have each been amended, claim 5 has been cancelled and new claims 39 and 40 have been added. No new matter has been added. It is respectfully submitted that this Amendment is fully responsive to the Office Action dated March 5, 2007.

Claim Objection:

Claim 1 stands objected due to the Examiner's assertion that "the same conducting layer" in claim 1 should be corrected to read as –a same conducting layer--. Accordingly, claim 1 has been amended as proposed by the Examiner. Thus, the present claim objection should be withdrawn.

Claim Rejections under 35 U.S.C. §112

Claim 28 stand rejected under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

This rejection is respectfully traversed.

The Examiner states that there is insufficient antecedent basis for the limitation: "the gate electrode" in claim 28 since there is two different gate electrodes required in the independent claim 1.

Claim 28 has been amendment such that original claim 28 is divided into claim 28 and 39. In claim 28, it is clarified that "the gate electrode" corresponds to a gate electrode of the third transistor. In claim 39, it is clarified that "the gate electrode" corresponds to a gate electrode of the fourth transistor. Thus, the claim rejections under 35 U.S.C. §112 should be withdrawn.

Claim Rejections under 35 U.S.C. §102

Claims 33 and 36 are rejected under 35 U.S.C. §102(e) as being anticipated by *Koizumi* (U.S. 7,081,607). This rejection is respectfully traversed.

The present invention has a feature that, in the image reading method for the solid-state image sensor, the photoelectric converts and the second transistors in all the rows are simultaneously reset, and the charges from the photoelectric converts is transferred simultaneously to the gate terminals of the second transistors via the first transistors in all the rows. As shown in, e.g., Figs. 6A and 6B of the present application, the photodiodes PD (photoelectric converters) and the floating diffusions (gate terminals of source follower transistors SF-Tr (second transistors)) in n^{th} and $n+1^{th}$ rows are simultaneously reset, after a

period of a photo detection time, charges are transferred from the photodiodes (photoelectric converters) to the gate terminals of the source follower transistors SF-Tr (second transistors) via the transfer transistors TG (first transistors) in all the rows, and signals and reset voltages in each of the rows are sequentially read.

On the other hand, in the image reading method of *Koizumi*, as shown, e.g., Fig. 13 and column 10, line 63 to column 11, line 38, a unit cell of the (n-1)-th row is reset by applying a control pulse ΦR1 to a reset switch Q2(n-1) (see column 10, lines 63-64), the transfer switch Q1(n-1) of the unit cell of the (n-1)-th row is turned on to transfer the optical signal by applying a control pulse ΦS2 (see column 11, lines 1-4), the optical signal of the (n-1)-th row is read out (see column 11, lines 4-7), a unit cell of the n-th row is reset by applying a control pulse ΦR2 to a reset switch Q2(n) (see column 11, lines 13-15), the transfer switch Q1(n) of the unit cell of the n-th row is turned on to transfer the optical signal by applying a control pulse ΦS3 (see column 11, lines 25-28), and then the optical signal of the n-th row is read out (see column 11, lines 29-38). That is, in *Koizumi*, the reset of the photoelectric converters and the amplifying transistor and the transfer of the optical signal of all the rows are performed not simultaneously but for each row. *Koizumi* neither teaches nor suggests that the reset of the photoelectric converters and the amplifying transistor and the transfer of the optical signal of all the rows are simultaneously performed.

Thus, *Koizumi* is clearly different from the present invention and does not provide any motivations for the present invention.

Claim Rejections under 35 U.S.C. §103

Claims 1, 5 and 28 stand rejected under 35 U.S.C. §103(a) as being unpatentable over *Koizumi* in view of *Guidash et al.* (U.S. 6,466,266). This rejection is respectfully traversed.

Claim 1 has been amended to include the features of cancelled claim 5. Amended claim 1 has a feature that the photoelectric converter and the first transistor are formed adjacent to each other in the row direction, the second transistor and the third transistor are formed adjacent to each other in the column direction, and the gate electrode of the first transistor and the gate electrode of the fourth transistor are extended in the column direction (see, e.g., Figs. 2 and 9).

The Examiner states that *Koizumi* discloses in Fig. 12 that the photoelectric converter and the first transistor are adjacent to each other in the row direction, the second transistor (Q3) and the third transistor (Q3) are adjacent to each other in the column direction, and the gate electrode of the first transistor (Q1 at line 16) and the gate electrode of the fourth transistor (Q4 at line 17) are extended in the column direction.

However, Fig. 12 of *Koizumi* is a circuit diagram of the solid-state image sensor. The circuit diagram is not for describing the positional relationships between the elements forming the solid-state image sensor (cell layout) but for describing the electrical connections between the elements forming the solid-state image sensor. The positional relationships between the elements forming the solid-state image sensor described in the circuit diagram have no meaning and do not always correspond to those in the cell layout. *Guidash et al.* discloses in Figs. 1b and 4 cell layouts of the solid-state image sensors. However, the cell layouts shown in Figs. 1b and 4

of *Guidash et al.* do not satisfy the relationships of claim 1. *Koizumi* and *Guidash et al.* neither teach nor suggest the positional relationships between the elements forming the solid-state image sensor as required in claim 1.

As described above, *Koizumi* and *Guidash et al.* are clearly different from the present invention and do not provide any motivations for the present invention. Thus, the present invention would have been unobvious to one of ordinary skill in the art, even though both of *Koizumi* and *Guidash et al.* are considered.

In view of the aforementioned amendments and accompanying remarks, Applicant submits that the claims, as herein amended, are in condition for allowance. Applicant requests such action at an early date.

If the Examiner believes that this application is not now in condition for allowance, the Examiner is requested to contact Applicant's undersigned attorney to arrange for an interview to expedite the disposition of this case. If this paper is not timely filed, Applicant respectfully petitions for an appropriate extension of time. The fees for such an extension or any other fees that may be due with respect to this paper may be charged to Deposit Account No. 50-2866.

Respectfully submitted,

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